MASTER OF SCIENCE
IN
ELECTRICAL ENGINEERING

THREE-DIMENSIONAL IMAGE SYNTHESIS: THEORY AND APPLICATION
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Inverse Synthetic Aperture Radar (ISAR) provides full range detection and classification of sea and air based targets through two-dimensional range-Doppler imaging. The Naval Postgraduate School has developed a custom integrated circuit that can simulate false ISAR images in order to fool enemy ISAR platforms. To validate specific hardware choices within this design, this thesis explores the effect on image quality of an overflow occurring within the final 16-bit summation adder of this circuit. Three solutions to the problem of overflows are presented and analyzed. The logical extension of ISAR development, that of three-dimensional target imaging, is next presented through the discussion of 3D monopulse radar, 3D interferometric ISAR, and a 3D, three-receiver ISAR. The relative strengths of each approach are compared, along with both MATLAB and X3D software models created for one specific 3D ISAR implementation. Through the superposition of 2D ISAR images, it is shown how 3D ISAR images may be created. Moreover, emphasis is placed on using this knowledge to both enhance current 2D ISAR techniques and to modify the false-target chip to handle 3D ISAR return signals. The thesis concludes with a study of Non-Uniform Rational B-Splines, through which the X3D software model was created.

KEYWORDS: Digital Image Synthesizer, DIS, ISAR, 3D ISAR, Adder Overflow Analysis, NURBS, X3D

AN EVALUATION OF ELECTRIC MOTORS FOR SHIP PROPULSION
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An evaluation was conducted of the various propulsion motors being considered for electric ship propulsion. The benefit of such an evaluation is that all of the propulsion options being considered by the U.S. Navy have been described in one document. The AC induction motor, AC synchronous motor, High Temperature Superconducting (HTS) motor and Superconducting DC Homopolar Motor (SDCHM) are examined. The properties, advantages, and disadvantages of each motor are discussed and compared. The power converters used to control large propulsion motors are also discussed. The Navy's IPS program is discussed and the results of concept testing are presented. Podded propulsion is introduced and the benefits are discussed. The final chapter presents the simulation results of a volts/Hertz controlled 30 MW induction motor. The evaluation revealed that the permanent magnet motor is the best propulsion motor when considering mature technology, power density, and acoustic performance. HTS motors offer significant volume reductions and improved acoustic performance as compared to conventional motors. This includes both AC and DC HTS motors. The main obstacle for the SDCHM remains the unavailability of high current capacity brushes.

KEYWORDS: Electric Propulsion, Electric Ship, Integrated Power System, Induction Motor, Permanent Magnet Motor, HTS Synchronous Motor, DC Homopolar Motor, Podded Propulsion

ELECTRICAL ENGINEERING

DESIGN, CONSTRUCTION AND TESTING OF A REDUCED-SCALE CASCADED MULTI-LEVEL CONVERTER

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The main focus in the design of the next generation combatant, DD(X), is the U.S. Navy's proposed Integrated Power System (IPS) which includes an all-electric propulsion drive system. The reduction of current waveform harmonics is critical in combatant propulsion systems such as the IPS. One method of reducing the current harmonics is to utilize a multi-level converter topology. The multi-level converter, as compared to a standard converter, features low dv/dt losses and low switching losses. This thesis examines the design, construction and testing of two multi-level converters operated in tandem, called a Cascaded Multi-Level Converter (CMLC). A digital logic switching circuit is designed and constructed to control the CMLC during the operational testing phase. The CMLC is demonstrated in a three-phase high-voltage configuration with 178.5 volts zero-to-peak voltage, 2.10 amps zero-to-peak current achieved using an R-L load.

KEYWORDS: DC-AC Converter, Multi-level Converter, Cascaded Multi-level Converter, Integrated Power System, DD(X)

DESIGN AND DEVELOPMENT OF A CONFIGURABLE FAULT TOLERANT PROCESSOR (CFTP) FOR SPACE APPLICATIONS

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The space environment has unique hazards that force electronic systems designers to use different techniques to build their systems. Radiation can cause Single Event Upsets (SEUs) which can cause state changes in satellite systems. Mitigation techniques have been developed to either prevent or recover from these upsets when they occur.

At the same time, modifying on-orbit systems is difficult in a hardwired electronic system. Finding an alternative to either working around a mistake or having to keep the same generation of technology for years is important to the space community. Newer programmable logic devices, such as Field Programmable Gate Arrays (FPGAs), allow for emulation of complex logic circuits, such as microprocessors. FPGAs can be reprogrammed as necessary, to account for errors in design, or upgrades in software logic circuits.

In an effort to provide one solution for both of these issues, this research was undertaken. The Configurable Fault Tolerant Processor (CFTP) emulates three identical processors, using Triple Modular Redundancy (TMR) to mitigate radiation hazards on a radiation tolerant FPGA. With the reconfigurable capabilities of FPGA technology, as newer processors can be emulated, these new configurations can be uploaded to the satellite as software code, thereby actually upgrading the processor in flight. This research used a 16-bit Reduced Instruction Set Computer (RISC) processor as its core. This thesis describes how the Harvard architecture of the processor interfaced with the Von Neumann architecture of the memory. It also explains the process by which errors are detected and corrected, as well as recorded.

KEYWORDS: Field Programmable Gate Array, FPGA, Fault Tolerant Computing, Single Event Upset, SEU, Commercial-off-the-Shelf Devices, COTS Devices

ELECTRICAL ENGINEERING

VHDL MODELING AND SIMULATION OF A DIGITAL IMAGE SYNTHESIZER FOR COUNTERING ISAR

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This thesis discusses VHDL modeling and simulation of a full custom Application Specific Integrated Circuit (ASIC) for a Digital Image Synthesizer (DIS). The DIS synthesizes the characteristic echo signature of a pre-selected target. It is mainly used against Inverse Synthetic Aperture Radars as an electronic counter measure. The VHDL description of the DIS architecture was exported from Tanner S-Edit, modified, and simulated in Aldec Active HDLTM. Simulation results were compared with C++ and Matlab simulation results for verification. Main subcomponents, a single Range Bin Processor (RBP), a cascade of four RBPs and a cascade of 16 RBPs were tested and verified. The overhead control circuitry, including Self Test Circuitry and Phase Extractor, was tested separately. Finally, the overall DIS was tested and verified using the control circuitry and a cascade of four RBPs together, representing the actual 512 RBPs. As a result of this research, the majority of the DIS was functionally tested and verified.

KEYWORDS: Digital Image Synthesizer, DIS, VLSI, ASIC, CMOS, VHDL, Active HDLTM, Aldec, Tanner

PERFORMANCE OF ACOUSTIC SPREAD SPECTRUM-SIGNALING IN SIMULATED OCEAN CHANNELS

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Direct-Sequence Spread Spectrum (DSSS) modulation is being advanced as the physical-layer basis for Seaweb undersea acoustic networking. DSSS meets the need for channel tolerance, transmission security, and multi-user access. This thesis investigates the performance of subspace-decomposition blind-equalization algorithms as alternatives to RAKE processing of DSSS signals. This approach is tailored for superior performance in time-dispersive and frequency-dispersive channels characteristic of ocean acoustic propagation. Transmitter and receiver structures are implemented in Matlab and evaluated with a statistics-based model of a doubly spread channel with additive noise. Receiver performance is examined using Monte Carlo simulation. Bit-error rates versus signal-to–noise ratio are presented for various multipath assumptions, noise assumptions, and receiver synchronization assumptions.

KEYWORDS: Acoustic Communications, Underwater Communications, Underwater Networks, Undersea Warfare, Statistics-based Channel Modeling, Direct-Sequence Spread-Spectrum, Blind Equalization, Subspace-Decomposition, DSSS, DS-CDMA, Telesonar, Seaweb

ELECTRICAL ENGINEERING

SHIPBOARD SENSOR CLOSED-LOOP CALIBRATION USING WIRELESS LANS AND DATA SOCKET TRANSPORT PROTOCOLS

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This thesis presents an application of wireless technology in a shipboard environment. The application is on developing a closed-loop shipboard sensor calibration system with two main objectives. The first objective is to reduce the personnel required to conduct a sensor calibration. The second objective is to reduce the time required to complete the calibration process. This is accomplished using wireless protocols and using technology that can be easily installed or used on United States Navy ships.

Using the DataSocket protocol, this thesis proves that pressure data that is wirelessly transmitted via IEEE 802.11b from a Network Capable Application Processor (NCAP) or Wireless LAN Input Output Node (W-LION) to an access point or gateway can be displayed on a wireless tablet computer. At the same time, the calibration standard being applied to the system is transmitted via Bluetooth to the wireless tablet computer. Both pressures are displayed simultaneously on the screen while the computer computes the difference and compares the sensor data versus an operator inputted tolerance. A green light indicates that the difference is within tolerance and a red light indicates that the difference is not within tolerance. The operator can then adjust the calibration constants on the tablet computer screen and watch the sensor data come within tolerance. Once the sensor data is within tolerance, the operator can write the constants wirelessly to the NCAP. This process reduces the number of personnel required to calibrate a sensor from two to one, and the time required by a factor of ten. It also helps the Navy facilitate condition based maintenance, assisting the United States Navy to move forward with initiatives that reduce manning and streamline processes.

KEYWORDS: Closed Loop Calibration, Wireless, Portable, Handheld, 802.11b, Bluetooth DataSocket

DESIGN AND SIMULATION OF A THREE-AXIS STABILIZED SATELLITE AND KALMAN FILTER RATE ESTIMATOR

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Design requirements for a small satellite (NPSat-1) Attitude Determination and Control Subsystem (ADCS) are a three-axis stabilized spacecraft which requires a control attitude of +/- 1.0 degrees and knowledge attitude of +/- 0.1 degree. Several design aspects are considered in development of attitude control systems for a small satellite: spacecraft dynamics, space environment, disturbance torques, orbit type, and spacecraft complexity. The ideal spacecraft's attitude sensor is a rate gyroscope, which provides rate information to the attitude control system. In the case of NPSat-1, due to budget constraints alternative sensors will be utilized: a three-axis magnetometer, earth sensors, and a Global Positioning System (GPS). A small satellite designed to have a three-axis stabilized, biased momentum system, must have a robust control system and requires a momentum wheel to provide stiffness to maintain attitude, and magnetic torque rods on each axis. The current design of NPSat-1 uses all of these sensors to provide rate information for damping and stability to the control system that requires a complicated attitude control design. The purpose of this attitude control design simulation is to investigate and propose a control law utilizing a single pitch momentum wheel and three magnetic torque rods. A further proposal is to utilize a constant speed momentum wheel to avoid momentum damping and over speed, replace the pitch control with magnetic torquers, and develop a Kalman filter estimator to provide all the required angular rates.

KEYWORDS: Kalman Filter, Molniya, MATLAB, SIMULINK, Three Axis Stabilization, Spacecraft, Satellite, Star Sensor, Estimation, Gyroscope, Rate

ELECTRICAL ENGINEERING

DC-DC POWER CONVERSION WITH GALVANIC ISOLATION
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As the Navy transitions to all electric warships, there will be many changes to the power distribution schemes found aboard ships today. It will be necessary to maintain reliability while supplying the various components onboard with the proper voltage levels. Since transformers cannot be used to alter voltage levels while providing galvanic isolation in DC power systems, it is necessary to find an efficient method to incorporate the increased safety provided by galvanic isolation in a DC power distribution system. This thesis examines the design and control of one possible element for a future Electrical Distribution System (EDS), a DC-DC converter with galvanic isolation. The main purpose of this study is to provide a working model with associated theoretical proof and simulations. MATLAB is used to provide observations of the converter's operation and the success of the control scheme implemented. Future work on this topic will be assisted by the inclusion of a parts list as well as recommendations for enhancing the prospects of this technology.

KEYWORDS: DC-DC Converter, Galvanic Isolation, Electrical Distribution System